UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/719,280	11/21/2003	Yuanning Chen	TI-35022.1	3187

23494 7590 03/21/2005

TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
CHEN, JACK S J	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 03/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/719,280	CHEN ET AL.	
	Examiner	Art Unit	
	Jack Chen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 9-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 9-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In response to the communication filed on March 3, 2005, claims 3, 9-11 are active in this application. Claims 1-2 and 4-7 were cancelled (see preliminary amendment dated on November 21, 2003).

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on March 3, 2005 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 3 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al., U.S./6,713,357 B1.

Wang et al. disclose an IC comprises a PMOS transistor (see abstract section, CMOS includes both PMOS and NMOS; also see col. 6, lines 17-25), said PMOS transistor having a gate insulator 5, wherein the gate insulator comprises of a nitride/oxide stacks (fig. 1B; col. 6, lines 27-31; in this case, the oxide layer of the gate insulator stacks is considered as the gate oxide), a lightly doped drain 7/8 coupled to said gate oxide (fig. 1B), and a cap layer 10 coupled to a majority of a top surface of said lightly doped drain but separated from said gate oxide (fig. 1B) by a layer of oxide 9 (fig. 1B) coupled to said lightly doped drain and a layer of nitride (i.e., the nitride of the nitride/oxide stacks) coupled to said lightly doped drain, said cap layer comprised of a high dielectric constant material (fig. 1B; col. 6, lines 46-50), see figs. 1A-4 and cols. 1-12 for more details.

3. Claims 3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kurimoto et al., U.S./5,221,632.

Kurimoto et al. disclose an IC comprises a PMOS transistor (see col. 7, lines 47-50, N-channel devices and P-channel devices), said PMOS transistor having a gate insulator 2, wherein the gate insulator comprises of a oxide/nitride/oxide stacks (fig. 3g; col. 7, lines 42-46; in this case, the lower oxide layer of the gate insulator stacks is considered as the gate oxide), a lightly doped drain 8 coupled to said gate oxide (fig. 3g), and a cap layer 5 (fig. 3g; col. 7, lines 35-41, i.e., Ta2O5) coupled to a majority of a top surface of said lightly doped drain but separated from said gate oxide by a layer of oxide 4 (fig. 3g or the upper oxide layer of the ONO stack) coupled to said lightly doped drain and a layer of nitride (i.e., the nitride of the oxide/nitride/oxide stacks) coupled to said lightly doped drain, said cap layer comprised of a high dielectric constant material (fig. 3g; col. 7, lines 35-41, i.e., Ta2O5), see figs. 1-7b and cols. 1-8 for more details.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 3, 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over En et al., U.S./6,764,966 B1.

En et al. Disclose an IC comprises a PMOS transistor (col. 5, lines 50-65), said PMOS transistor having a gate oxide 20 (fig. 1), a lightly doped drain 14/16 coupled to said gate oxide (fig. 1), and a cap layer 28/30 (fig. 1, wherein the cap layer is part of the graded dielectric constant spacers 24, which includes layers 26, 28, 30 and 32) coupled to a majority of a top surface of said lightly doped drain but separated from said gate oxide (fig. 1), said cap layer comprised of a high dielectric constant material (fig. 1), see figs. 1-13 and cols. 1-14 for more details. En et al. disclose using a plurality of high-k materials for the graded dielectric constant

spacers, wherein the dielectric constant of the graded dielectric constant spacers decrease in a direction away from the sidewalls of the gate (i.e. abstract) and the spacer ends with a layer of material having a dielectric constant less than the preceding layer (i.e., col. 5, lines 1-5). En et al. disclosed above, and in particular col. 6, lines 58-67 shows one of the available high-k dielectric material is hafnium silicon oxynitride, which has the K value of about 16; col. 7, line 1 shows another available high-k dielectric material, such as hafnium silicon nitride, which has the K value of about 18 and col. 7, table 1 shows the K values for other high-k dielectric materials, such as titanium dioxide (k value of about 30) and tantalum oxide (k value of about 26). Although En et al. does not explicitly state using hafnium silicon oxynitride for layer 30 (fig. 1) in the related text, but it appears that using hafnium silicon oxynitride for layer 30, hafnium silicon nitride for layer 28 and titanium dioxide for layer 26 are Prima Facie obvious over En et al since this will form the graded dielectric constant spacers.

7. Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wang et al., U.S./6,713,357 B1 in view of Xiang et al., U.S./6,657,267 B1.

Wang et al. Disclosed above in paragraph 2, and in particular Col. 6, lines 45-48 shows using any high-k dielectric material for the cap layer 10 (i.e., with k greater than 3.9). Although Wang et al. does not explicitly state using hafnium silicon oxynitride as the cap layer in the related text, it appears that using hafnium silicon oxynitride as the cap layer is Prima Facie obvious over Wang et al since the hafnium silicon oxynitride has dielectric constant greater than 3.9. Furthermore, Xiang et al. also teach a semiconductor device having hafnium silicon oxynitride as the high-k dielectric material (see cols. 5-6, table 1), see figs. 1-3C and cols. 1-10 for more details.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jack Chen whose telephone number is (571)272-1689. The examiner can normally be reached on Monday-Friday (9:00am-6:30pm) alternate Monday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead can be reached on (571)272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jack Chen
Primary Examiner
Art Unit 2813

March 16, 2005